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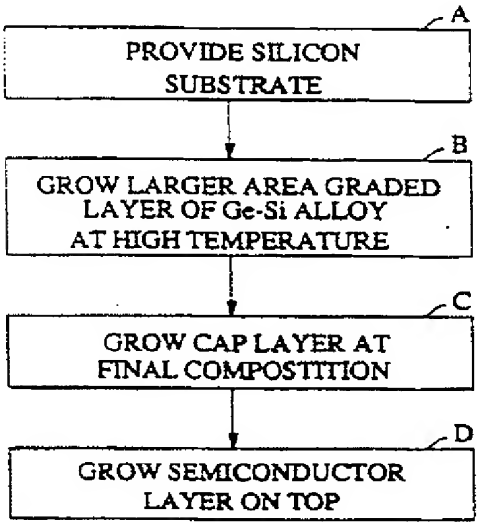
(54) Method for making low defect density semiconductor heterostructure and devices made thereby.

(57) Applicants have discovered that by growing germanium-silicon alloy at high temperatures in excess of about 850° C and increasing the germanium content at a gradient of less than about 25% per micrometer, one can grow on silicon large area heterostructures of graded Ge_xSi_{1-x} alloy having a low level of threading dislocation defects. With low concentrations of germanium ($.10 \leq x \leq .50$), the heterolayer can be used as a substrate for growing strained layer silicon devices such as MODFETS. With high concentrations of Ge ($.65 \leq x \leq 1.00$) the heterolayer can be used on silicon substrates as a buffer layer for indium gallium phosphide devices such as light emitting diodes and lasers. At concentrations of pure germanium ($X=1.00$), the heterolayer can be used for GaAs or GaAs/AlGaAs devices.

FIG. 1



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EUROPEAN SEARCH REPORT

Application Number
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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	US-A-3 935 040 (D.R.MASON) * column 2, line 67 - column 3, line 10 * * claims 1,2 *	1,7	H01L21/20 H01L21/335 H01L33/00 H01L21/82 H01L29/76
A	JOURNAL OF APPLIED PHYSICS vol. 59, no. 11 , June 1986 , NEW YORK US pages 3756 - 3759 M.S.COOK 'LATTICE-GRADED EPITAXIAL LAYERS' * page 3758, column 1, paragraph 1 - column 2, paragraph 3 *	1,5,7,9	
A	SOLAR CELLS vol. 20, no. 3 , April 1987 , LAUSANNE CH pages 237 - 243 S.S.CHU ET AL. 'THIN FILM GAAS SOLAR CELLS ON GERMANIUM-COATED SILICON SUBSTRATESBY CHEMICAL VAPOR DEPOSITION' * page 238, paragraph 3 - page 239, paragraph 2 *	1,5,7,9	
A	PATENT ABSTRACTS OF JAPAN vol. 6, no. 128 (E-118)(1006) 14 July 1982 & JP-A-57 053 927 (OKI DENKI KOGYO K.K.) 31 March 1982 * abstract *	4	TECHNICAL FIELDS SEARCHED (Int.Cl.5) H01L
A	EP-A-0 228 516 (LICENTIA PATENT-VERWALTUNGS-GMBH) * page 3, line 13 - page 4, line 32 *	1,3,11	
A	TECHNICAL DIGEST OF INTERNAL ELECTRON DEVICES MEETING 9 December 1990 , SAN FRANCISCO US pages 375 - 378 E.MURAKAMI ET AL. 'ULTRA HIGH HOLE MOBILITY IN STRAIN- CONTROLLED SI-GE MODULATION-DOPED FET' *WHOLE ARICLE*	3,11	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	2 May 1994	Schuermans, N

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 92 30 3475

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	EP-A-0 307 850 (LICENTIA PATENT-VERWALTUNGS-GMBH) * column 4, line 26 - column 6, line 5 *	12	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

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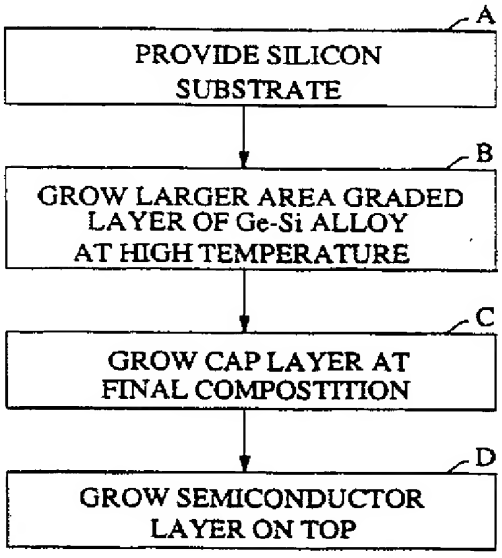
FIG. 1



EP 0 514 018 A2

Field of the Invention

This invention relates to a method for making a semiconductor heterostructure of germanium-silicon alloy that has low threading dislocation density in the alloy layer and to devices made thereby. Such low defect structures are particularly useful as buffer layers for making semiconductor devices comprising indium gallium phosphide, gallium arsenide or strained layers of silicon.

Background of the Invention

There is considerable interest in heterostructure devices involving greater epitaxial layer thickness and greater lattice misfit than present technology will allow. For example, it has long been recognized that germanium-silicon alloy Ge_xSi_{1-x} grown on silicon substrates would permit a variety of optoelectronic devices, such as LEDs, marrying the electronic processing technology of silicon VLSI circuits with the optical component technology available in direct band semiconductors. Indeed, it has been proposed that an intermediate epitaxial layer of germanium-silicon alloy would permit the epitaxial deposition of gallium arsenide overlying a silicon substrate and thus permit a variety of new optoelectronic devices using silicon electronic components and gallium arsenide optical components. However, despite the widely recognized potential advantages of such combined structures and despite substantial efforts to develop them, their practical utility has been limited by high defect densities in heterostructure layers grown on silicon substrates.

Dislocation defects partition an otherwise monolithic crystal structure and introduce unwanted and abrupt changes in electrical and optical properties. Dislocation defects arise in efforts to epitaxially grow one kind of crystalline material on a substrate of a different kind of material due to different crystal lattice sizes of the two materials. Dislocations form at the mismatched interface to relieve the misfit strain. Many of the misfit dislocations have vertical components, termed threading segments, which extend at a slant angle through any subsequent layers. Such threading defects in the active regions of semiconductor devices seriously degrade device performance.

A variety of approaches have been used to reduce dislocations with varying degrees of success. One approach is to limit the heterolayer to a thin layer of material that has a lattice crystal structure closely matching the substrate. Typically the lattice mismatch is within 1% and thickness of the layer is kept below a critical thickness for defect formation. In such structures, the substrate acts as a template for growth of the heterolayer which elastically conforms to the substrate template. While this approach eliminates dislocations in a number of structures, there are relatively few near lattice-matched systems with large energy band offsets. Thus with this approach the design options for new devices are limited.

A second approach set forth in the copending application of E. A. Fitzgerald, Serial No. 07/561744 filed August 2, 1990, utilizes heterolayers of greater thickness but limited lateral area. By making the thickness sufficiently large as compared with the lateral dimension, threading dislocations are permitted to exit the sides of layer. The upper surface is thus left substantially free of defects. This approach permits the fabrication of a variety of devices and circuits which can be made on limited area surfaces having an area of less than about 10,000 square micrometers

A third approach is to deposit successive layers of germanium-silicon alloy on a silicon substrate, increasing the germanium content with each successive layer. The goal is to avoid dislocations by spreading the strain among successive layers. Unfortunately this approach has not worked. For example, it has been found that step grading 20% Ge over 2000 angstroms to produce pure Ge results in substantially the same high dislocation density as depositing pure Ge on Si. See J. M. Baribeau et al., 63 Journal of Applied Physics 5738 (1988). Applicants believe that this approach fails because at conventional growth temperatures --typically about 550° C-- the initial layer of Si-Ge is almost entirely elastically strained. Thus when the next layer of Si-Ge with greater germanium content is applied, the mismatch between the two Si-Ge layers is nearly that between the initial Si-Ge layer and the Si substrate, resulting in high dislocation density. Accordingly, there is a need for a method of making large area, low defect heterostructures on silicon.

Summary of the Invention

Applicants have discovered that by growing germanium-silicon alloy at high temperatures in excess of about 850° C and increasing the germanium content at a gradient of less than about 25% per micrometer, one can grow on silicon large area heterostructures of graded Ge_xSi_{1-x} alloy having a low level of threading dislocation defects. With low concentrations of germanium ($.10 \leqq x \leqq .50$), the heterolayer can be used as a substrate for growing strained layer silicon devices such as MODFETS. With high concentrations of Ge ($.65 \leqq x \leqq 1.00$) the heterolayer can be used on silicon substrates as a buffer layer for indium gallium phosphide devices such

as light emitting diodes and lasers. At concentrations of pure germanium (X=1.00), the heterolayer can be used for GaAs or GaAs/AlGaAs devices.

Brief Description of the Drawing

In the drawings:

FIG. 1 is a block diagram illustrating the method of making a low defect density semiconductor heterostructure.

FIG. 2 is a schematic cross section of a strained silicon layer MODFET;

FIG. 3 is a schematic cross section of an indium gallium arsenide surface emitting LED; and

FIG. 4 is a schematic cross section of a gallium arsenide LED with integrated drive transistor.

It is to be understood that these drawings are not to scale.

Detailed Description

Referring to the drawings, FIG. 1 is a flow diagram illustrating the process for making a low defect density semiconductor heterostructure in accordance with the invention. As shown, the first step is providing a silicon substrate. Preferably the substrate is a standard (100) oriented silicon wafer of the type typically used in the fabrication of integrated circuits. Advantageously, as a preliminary step, the substrate is provided with one or more large area recessed tubs by conventional photolithographic patterning and etching. The tubs can have an area in excess of 12,000 square micrometers and a depth of several micrometers, depending upon the thickness of germanium-silicon alloy to be grown. The objective is to provide a tub of proper depth so that a germanium-silicon alloy layer grown in the tub will be substantially coplanar with the non-recessed portion of the silicon substrate.

The second step of the process is to grow at high temperature on the silicon substrate a large area, graded layer of germanium-silicon alloy, Ge_xSi_{1-x}. The growth process is preferably chemical vapor deposition (CVD) or molecular beam epitaxy (MBE). The substrate growth starting temperature should be in the range 850° C - 1100° C, and the area of the graded alloy can exceed 12,000 square micrometers. The starting composition is preferably pure silicon. Germanium is introduced to form Ge_xSi_{1-x} at a gradient of less than about 25% per micron. Preferably the grading is linear at a rate of about 10% per micron. Alternatively the grading can be stepwise at similar gradients. As the germanium content of the alloy increases, the growth temperature is advantageously scaled down in proportion to the reduced melting temperature of the alloy. The objective is to avoid melting the alloy. Graded growth of Ge_xSi_{1-x} is continued until a desired final composition is reached.

The choice of final composition depends upon the intended use of the heterostructure. If, for example, the structure is to be used as a substrate for growing a strained layer silicon device, the final Ge concentration should fall within the range of 10-50%. If the structure is to be used as a substrate for an indium gallium phosphide device, the final Ge concentration should fall within the range of 65-100%. On the other hand, if the structure is to be used as a substrate for GaAs or GaAs/AlGaAs devices, the Ge concentration is preferably about 100%.

After the desired final composition is reached, an optional cap layer with the same final composition can be grown on the graded layer to a thickness in excess of 100 angstroms and preferably in excess of one micrometer. The effect of the cap layer is to further relax the low level of residual strain at the top of the graded layer.

The fabrication and structure can be understood in greater detail by consideration of the following specific examples.

Example 1: Heterostructure Substrate (MBE)

A (100) oriented silicon substrate is provided with a large area rectangular tub approximately ten micrometers deep by covering the major surface with a masking layer of silicon oxide, etching a rectangular opening in the oxide mask to define the periphery of the tub, and then etching the exposed silicon with ethylene-diamine-pyrocatechol (EDP). The EDP etch produces smooth tub surfaces with sidewalls in the (111) planes of the silicon substrate. The substrate is then cleaned with a 3:1 mixture of H_2SO_4 and H_2O_2 for ten minutes and with buffered HF for 1 minute.

The cleaned substrate is placed in a Riber EVA 32 Silicon MBE Apparatus controlled by a Sentinel 3 Deposition Rate Controller. The chamber is evacuated to a pressure of less than 10^{-9} Torr, and any oxide on the tub surfaces is dissociated by heating the substrate to about 800° C and applying a low flux silicon beam at a rate of about 0.05 angstrom/s. Silicon growth at higher rate is continued to a thickness of about 0.1 micrometer

to form a silicon buffer layer.

After formation of the buffer layer, the substrate temperature is increased to about 900° C and the graded layer is grown. Graded growth is begun with pure silicon at a rate of about 3 angstroms per second. The total growth rate is kept constant while introducing germanium at a linear gradient of about 10% per micrometer. The objective is to keep growth near thermal equilibrium. The parameter variations for graded growth to 100% germanium at 10% per micrometer grading are set forth in the Table 1, giving thickness, percent of Germanium, temperature and current rates at various times into growth.

Table 1

PARAMETER VARIATIONS FOR 10%/micron GRADING

Starting Rates (Sentinel): Si/Ge = 67.8/0.5

time into growth (min)	t(μ)	Ge%	liquidus (C/K)	%T	T substrate (C)	Current Rates (Sentinel): Si/Ge
0	0	0	1414/1687	100	900	67.8/0.5
27	0.486	5	1402/1675	99.3	892	64.4/3.5
54	0.972	10	1390/1663	98.6	884	61.0/6.7
81	1.458	15	1375/1648	97.7	873	57.6/10.5
108	1.944	20	1362/1635	96.9	864	54.2/14.0
135	2.430	25	1350/1623	96.2	855	50.9/17.5
162	2.916	30	1335/1608	95.3	845	47.5/21.0
189	3.402	35	1320/1593	94.4	834	44.1/24.5
216	3.888	40	1305/1578	93.5	824	40.7/28.0
243	4.374	45	1290/1563	92.6	813	37.3/31.5
270	4.860	50	1270/1543	91.5	800	33.9/34.9
297	5.346	55	1255/1528	90.6	790	30.5/38.4
324	5.832	60	1235/1508	89.4	776	27.1/41.9
351	6.318	65	1210/1483	87.9	758	23.7/45.4
378	6.804	70	1185/1458	86.4	740	20.3/48.9
405	7.290	75	1160/1433	84.9	722	17.0/52.4
432	7.776	80	1130/1403	83.2	703	13.6/55.9
459	8.262	85	1100/1373	81.4	681	10.2/59.4
486	8.748	90	1055/1328	78.7	650	6.8/62.9
513	9.234	95	1010/1283	76.0	618	3.4/66.4
540	9.720	100	938/1211	71.8	569	0.5/69.9

After 100% germanium is reached, a final germanium cap layer having a thickness in the range between 1000 angstroms and one micrometer is grown on top.

Structures with less than 100% germanium can be obtained by terminating graded growth at the desired germanium concentration and growing the final cap layer at that concentration.

Example 2: Heterostructure Substrate (CVD)

As preliminary steps, a 100 mm (100) Si wafer was cleaned in dilute HF (1% in H_2O) and spin-dried in N_2. The wafer was loaded into an RTCVD reactor and pumped down to a base pressure of 10^{-7} Torr. The wafer was heated to 1000° C for 15 seconds in flowing H_2 (3 lpm) to remove residual oxygen and carbon, and then cooled in 2 seconds to 900° C.

After these preliminary steps, deposition was commenced by depositing a Si buffer approximately 1000 Å thick. This was accomplished using SiH_2Cl_2 (1% in H_2, 1 lpm) for 1 minute at a pressure of about 4 Torr. Immediately thereafter, GeH_4 (1% GeH_4 in H_2) was introduced gradually to create a Si-Ge alloy layer that increased from 0 to 50% Ge. The GeH_4 flow can be increased by 4 sccm flow increments every 40 seconds. The SiH_2Cl_2 was decreased by the same flow increment in the same time scale; thus, the total GeH_4 and SiH_2Cl_2 flow was maintained at 1 lpm. Deposition at 900° C resulted in a Si-Ge graded alloy layer that continually relaxed as it was grown.

Heterostructures fabricated as described in Examples 1 and 2 demonstrate a reduction in defects as compared with conventionally fabricated heterostructures. Triple crystal X-ray diffraction shows that for 0. 10 <x< 0.50, the layers are totally relaxed. The Ge_xSi_{1-x} cap layers, when examined by plan-view and cross-sectional transmission electron microscopy are threading dislocation free. Electron beam induced current images revealed low threading dislocation densibes of $4x10^5 \pm 5x10^4$ cm^{-2} for X=0.25 and $3x10^6 \pm 2x10^6$ cm^{-2} for x=0.50. Photoluminescence spectra from the cap layers are substantially identical to photoluminescence from bulk Ge_xSi_{1-x}.

These low defect heterostructures can serve as buffer layers for epitaxially growing a wide variety of devices varying from those employing strained layer of silicon to those employing III-V semiconductors.

FIG. 2 is a schematic cross section of a device employing a low defect heterostructure to produce a strained silicon MODFET. In essence the MODFET is fabricated on a heterostructure comprising a Ge_xSi_{1-x} cap layer 1 grown on a graded layer 2, all disposed on a silicon substrate 3. The heterostructure is fabricated as described above, with a maximum concentration of germanium in the range ($0.10 \leq x \leq 0.50$) and preferably with x=0.30.

The MODFET fabricated on the heterolayer comprises, in essence, a strained layer of silicon 4 epitaxially grown on layer 1. Another layer 5 of Ge_xSi_{1-x} (initially intrinsic but n-doped after 50 to 900 angstroms) is grown over the silicon and, n^+ spaced apart contact regions 6A and 6B are formed to contact the strained silicon layer 4. Ohmic contacts 8A and 8B are made with the n^+ contact regions 6A and 6B, and a Schottky barrier contact 7 to layer 5 is disposed between the spaced apart ohmic contacts. A dielectric layer 9 advantageously separates the contacts 7, 8A, and 8B.

Silicon layer 4 preferably has a thickness in the range 100 angstroms to 1000 angstroms and is preferably undoped.

Ge_xSi_{1-x} layer 5 preferably has a thickness in the range 50 angstroms to 1000 angstroms. Layer 5 is preferably intrinsic for 50 to 900 angstoms and then n^+ doped with antimony, phosphorus or arsenic to a concentration in the range $1x10^{17}/cm^3$ - $5x10^{18}/cm^3$. Layer 5 preferably has a concentration of Ge not less than that of cap layer 1.

The n^+ contact regions 6A and 6B are preferably formed by implanting antimony, arsenic or phosphorus to silicon layer 4 at a concentration of $10^{19}/cm^3$. The ohmic contacts 8A and 8B can be layers of aluminum and the Schottky contact 7 can be a layer of platinum.

The resulting MODFET acts as a field effect transistor with the advantage of higher speed. The application of a signal voltage bias to the Schottky contact 7 (commonly known as the gate) changes the electron density inside the Si layer 4, which in turn changes the sheet conductance of the channel between 8A and 8B and results in transistor action. The strained silicon layer is a particularly high speed path for at least three reasons: 1) the stralning of the silicon alters the energy bands of the silicon to favor conduction by low effective mass, high mobility electrons, 2) the silicon layer is free of impurities to interfere with electron flow, and 3) the silicon layer grown on a low defect substrate has a low concentration of defects to interfere with electron flow.

FIG. 3 is a schematic cross section of an Indium gallium arsenide surface emitting LED fabricated on a heterolayer. Specifically, the LED 20 is fabricated on a heterostructure comprising a Ge_xSi_{1-x} layer 12 grown within a large area tub 11 on a silicon substrate 10. The heterostructure is fabricated essentially as described above, except that the Ge_xSi_{1-x} is doped with p-type impurities, such as Be, to a concentration of $10^{18}cm^{-3}$.

The LED 20 is fabricated on the Ge_xSi_{1-x} using conventional processes such as chemical beam epitaxy to form the constituent layers 21-25 whose thicknesses, constituency and doping are set forth in table 2 below:

Table 2

Layer No.	Composition	Thickness	Dopant	Concentration
21	$In_y(Ga_{1-z}Al_z)_{1-y}P$	1 micrometer	n^+(Si)	$10^{18}cm^{-3}$
22	$In_w(Ga_{1-x}Al_x)_{1-w}P$	0.5 micrometer	n(Si)	$10^{17}cm^{-3}$
23	$In_u(Ga_{1-v}Al_v)_{1-u}P$	0.2 micrometer	none	intrinsic
24	$In_w(Ga_{1-x}Al_{x)_{1-w}}P$	0.5 micrometer	p(Be)	$10^{17}cm^{-3}$
25	$In_y(Ga_{1-z}Al_z)_{1-y}P$	1 micrometer	p^+(Be)	$10^{18}cm^{-3}$

After the constituent layers are grown, the next step is to form ohmic contacts and to isolate the device. Ohmic contact 26 is formed to contact p-doped layer 25 by depositing a layer of gold-zinc alloy and photolithographically patterning the metal to form a annular ring.

To isolate the diode, the portion of layers 22-25 outside the metal contact ring 26 can be etched away. Using a photoresist circle as a mask, a mesa is etched around ring 26 terminating on n-doped layer 21. Preferably etching is by reactive ion etching in order to obtain a mesa with vertical side walls around the periphery of ring 26.

Next ohmic contact 27 is made with the now exposed n-doped layer 21 as by depositing a layer of gold-germanium alloy and photolithographically defining annular contact ring 27 around the mesa. For further isolation, a mesa concentric with ring 27 can be chemically etched through layer 21.

The final steps involve depositing passivating insulating layers 28 and forming metal interconnects 29 to contacts 26 and 27 in accordance with techniques well known in the art. The interconnects can advantageously extend to integrated electronic circuitry (not shown) formed on the silicon substrate.

In operation, a DC bias voltage applied between contacts 26 and 27 induces emission of light through the center of ring 26.

A particular advantage of this embodiment is that the composition of the Ge_xSi_{1-x} layer can be chosen to lattice match a variety of indium gallium phosphide compounds giving a wide choice of emission wavelengths. For example, when the indium gallium phosphide compound matches a Ge-Si buffer with 65-70% Ge, the emission is been whereas a compound lattice matched to 100% Ge emits red. Thus much of the visible range can be covered.

FIG. 4 is a schematic cross section of a GaAs surface emitting LED fabricated on a heterolayer. In particular, the LED 30 is fabricated on a heterostructure comprising a Ge_xSi_{1-x} layer 12 grown within a large area tub 11 on a silicon substrate 10. In addition the LED is shown connected via a metal lead 36 to a drive transistor 40 integrally formed in silicon substrate 10.

The Ge_xSi_{1-x} layer is formed in tub 11 as described in Example 1 above. The Ge_xSi_{1-x} is preferably undoped and achieves a final composition consisting essentially of pure germanium in order to lattice match the materials of LED 30.

LED 30 comprises a layer of n-doped $Al_yGa_{1-y}As$ 31 grown on the Ge surface, as by MBE, a layer of p-doped GaAs 32 grown on layer 31 and a layer 33 of p^+ doped $Al_yGa_{1-y}As$ grown on layer 32. The LED has an annular p-type ohmic contact 34 to layer 33 and an n-type ohmic contact 35 to layer 31.

In a specific structure, n-layer 31 can be doped with silicon to a concentration of $10^{18}/cm^3$ and have a thickness of 0.5 micrometer, p-layer 32 can be doped with Be to a concentration of $10^{16}/cm^3$ and have a thickness of 0.6 micrometer. P+ layer 32 can be doped with Be to $10^{19}/cm^3$ and have a thickness of 0.5 micrometers. The n-contact 35 can be a composite layer of nickel, titanium and gold, and the p-contact 34 can be AuBe alloy.

The LED 30 can be connected to transistor 40 with aluminum interconnects 36.

Drive transistor 40 consists essentially of an n-type emitter 41, a p-type base 42 and an n-turn collector 43 integrally fabricated on silicon substrate 10 in accordance with conventional techniques well known in the art.

This example illustrates the important advantage that the invention permits silicon electronic components (e.g. transistor 40) and III-V semiconductor optical components (e.g. LED 30) to be fabricated on the same substrate. Clearly, much more complex circuits can be fabricated on the structure.

Claims

1. A method for making a semiconductor device comprising the steps of:
providing a monocrystalline silicon substrate
epitaxially growing on said silicon substrate at a temperature in excess of 850° C a graded layer of Ge_xSi_{1-x} with increasing germanium content at a gradient of less than about 25% per micrometer,
epitaxially growing a layer of semiconductor material above said graded layer of Ge_xSi_{1-x}.

2. The method of claim 1 wherein said layer of semiconductor material comprises a cap layer of Ge-Si alloy having the same composition as the surface of the graded layer and a thickness in excess of 100 angstroms.

3. The method of claim 1 wherein said graded layer of Ge_xSi_{1-x} has a final composition in the range $0.1 \leqq x \leqq 0.5$ and said layer of semiconductor material comprises silicon.

4. The method of claim 1 wherein said graded layer of Ge_xSi_{1-x} has a final composition in the range ($0.65 \leqq x \leqq 1.0$) and said layer of semiconductor material comprises indium gallium phosphide.

5. The method of claim 1 wherein said graded layer of Ge_xSi_{1-x} has a final composition of pure germanium and said layer of semiconductor material comprises gallium arsenide or aluminum gallium arsenide.

6. The method of claim 1 wherein said epitaxial layers are grown by molecular beam epitaxy.

7. The method of claim 1 wherein said epitaxial layers are grown by chemical vapor deposition.

8. The method of claim 1 further comprising the step of providing said silicon substrate with a recessed tub having a depth equal to the sum of the thickness of the graded layer of Ge_xSi_{1-x} and the cap layer.

9. The method of claim 1 wherein the temperature of growth of said graded layer of Ge_xSi_{1-x} is scaled in proportion to the melting temperature of the Ge_xSi_{1-x}.

10. The method of claim 1 wherein the area of said graded Ge_xSi_{1-x} layer exceeds 12,000 square microns.

11. A MODFET device comprising
a layer of germanium-silicon alloy having germanium concentration in the range between 10 percent and 50 percent;
a layer of strained silicon epitaxially grown on said layer of alloy;
a second layer of germanium-silicon alloy epitaxially grown on said strained silicon layer, said second layer including donor dopants and spaced apart contact regions for electrically contacting said silicon layer;
source and drain ohmic contacts means disposed on said second layer of alloy for contacting said contact regions
Schottky barrier contact means disposed between said source and drain contact means, whereby conduction between said source and drain is enhanced by application of a negative voltage to said Schottky contact.

12. A device comprising:
a layer of germanium-silicon alloy Ge_xSi_{1-x} ($0.10 \leqq x \leqq .50$) having a threading dislocation density of less than $5x10^6 cm^{-2}$;
a strained layer of silicon epitaxially grown on said layer of alloy;

a second layer of germanium-silicon alloy epitaxially grown on said strained layer of silicon; and means for making electrical contact with spaced apart regions of said strained silicon layer.

13. A device according to claim 12 wherein said strained layer of silicon is undoped.

14. A device according to claim 12 wherein at least one of said layers of germanium-silicon alloy is n-doped.

FIG. 1

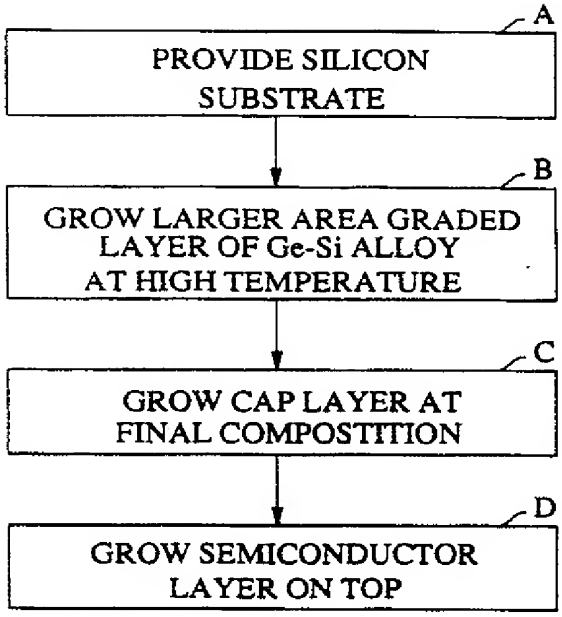

A
PROVIDE SILICON SUBSTRATE
B
GROW LARGER AREA GRADED LAYER OF Ge-Si ALLOY AT HIGH TEMPERATURE
C
GROW CAP LAYER AT FINAL COMPOSTITION
D
GROW SEMICONDUCTOR LAYER ON TOP

FIG. 2

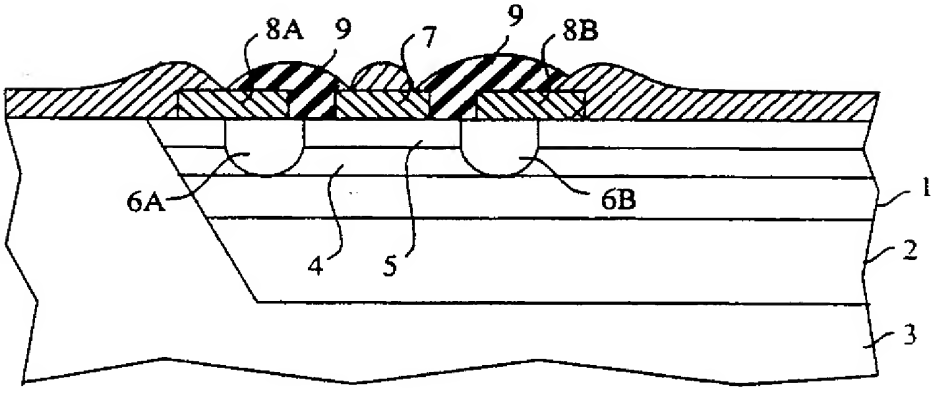

8A
9
7
9
8B
6A
6B
4
5
1
2
3

FIG. 3

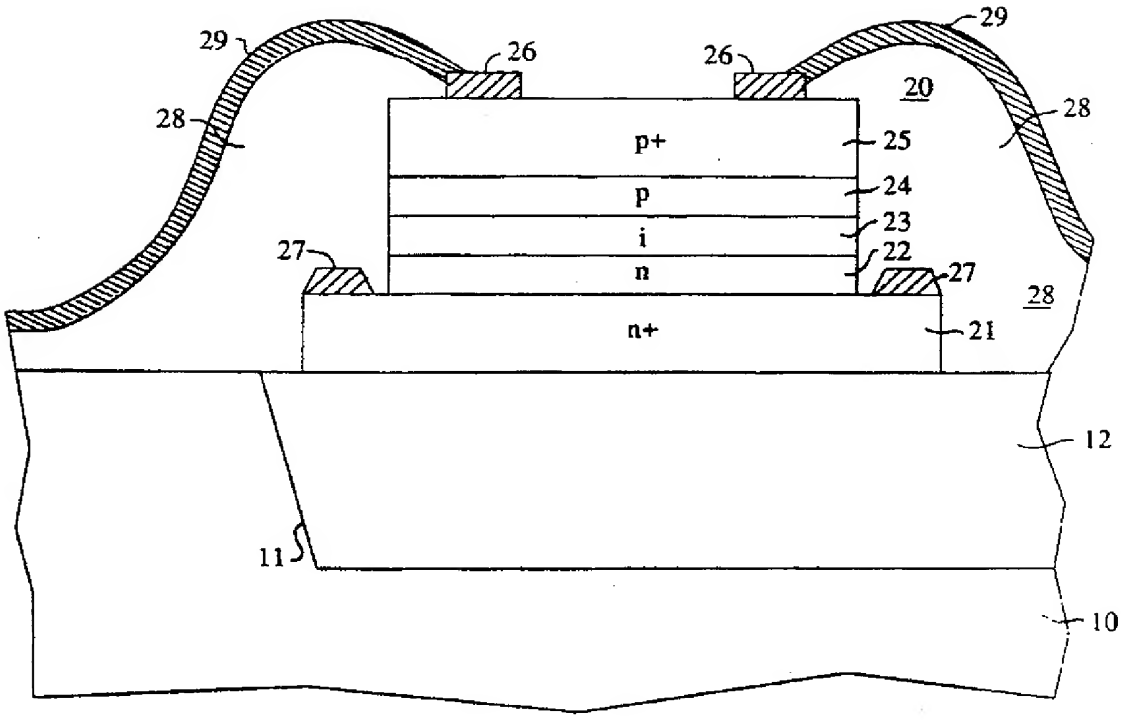
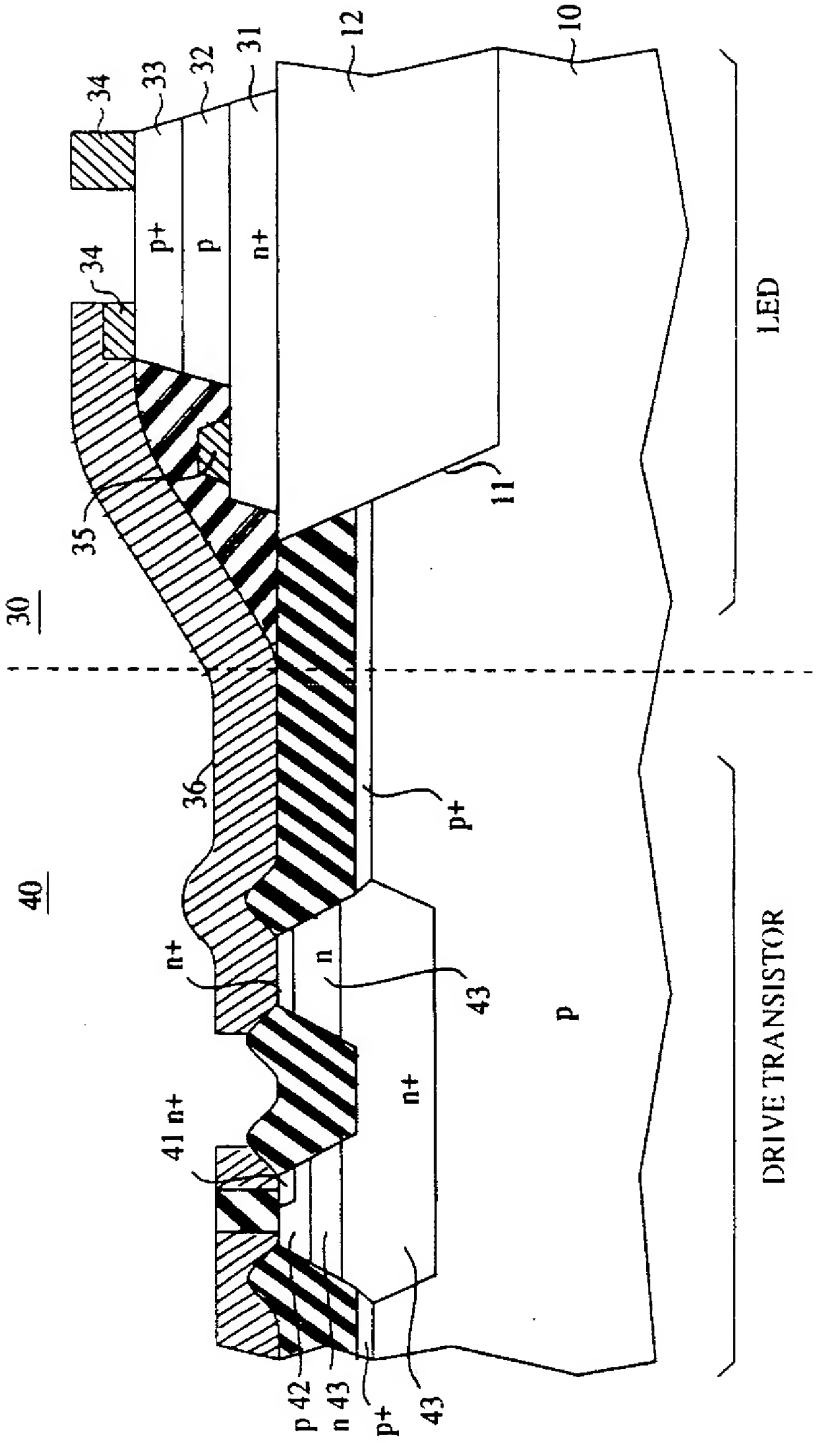


FIG. 4


30
40
LED
DRIVE TRANSISTOR
10
11
12
31
32
33
34
34
35
36
p+
p
n+
p+
n+
n
43
p
n+
41 n+
p 42
n 43
p+
43